The MITRE Tactical Channel Emulation System

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***Abstract*—We present a robust solution to the problem of predicting and evaluating the performance of fielded tactical radios. The MITRE Tactical Channel Emulation System (TCES) enables the evaluation of networked radios in a laboratory environment using digital baseband emulation of RF propagation conditions. The digital emulation approach offers significant advantages (e.g., cost, logistics, repeatability, etc.) over field testing. Furthermore, digital emulation is preferable to a purely software-based simulation approach in that it offers a high degree of accuracy and precision in radio behavior and can operate in real time. This approach also offers improvements in fidelity and scale over existing analog-based radio testing systems. A scenario encompassing multiple radios that are either stationary or are placed on some arbitrary combination of mobile platforms in a chosen geographical area can be readily constructed using an appropriate front-end modeling tool. The propagation information (e.g., time-varying and position-dependent path loss and carrier phase rotation) is extracted from the front-end tool and is used to control a matrix of Field-Programmable Gate Array (FPGA) based digital baseband channels. Each radio transmitter output is captured in real time, converted to a digital baseband signal, and passed through a digital baseband channel. The signal for each radio receiver is comprised of a linear combination of these digital baseband channel outputs. Each linear combination of channel outputs is converted to an analog RF signal and forms the input signal for a given radio receiver. An initial 16 x 16 channel prototype of this system has already been used successfully by a DoD customer, and we discuss extensions to the system, such as 32 x 32 and 64 x 64 channel configurations, along with enhancements such as Doppler and multipath channels.**

Keywords—Tactical radios, channel emulation, RF propagation, Doppler, multipath, FPGA, modeling, simulation, MANET.

I. INTRODUCTION

The characterization of modern tactical radios and their associated waveforms and mobile ad-hoc networking (MANET) algorithms involves significant challenges in terms of the number of radios that must be tested simultaneously and the variety of RF propagation conditions that must be considered. The MITRE Tactical Channel Emulation System (TCES) enables the evaluation of networked radios in a laboratory environment using realistic digitally emulated propagation conditions. The use of a laboratory-based digital emulation approach has multiple significant advantages. Test scenarios associated with tactical radio waveforms may involve up to 100 individual radio nodes [1, 2]. Performing these tests in a laboratory setting avoids the cost and logistic challenges of field testing and also enables a level of repeatability that would otherwise not be attainable. Further, a digital hardware-based implementation provides real-time operation not obtainable with a purely software-based system. Finally, although various existing commercial off-the-shelf (COTS) products provide limited combinations of the above-mentioned benefits, our system is novel in that it eliminates the calibration challenges and attenuation-only operation of purely analog systems while incorporating high-fidelity channel models in a scalable architecture not present in existing digital systems.

Our system leverages the extensive capabilities of modern RF propagation modeling tools such as AGI STK, Remcom Wireless InSite, and custom DoD simulation environments. Using one of these front-end modeling tools, a scenario encompassing multiple radios that are either stationary or are placed on some arbitrary combination of mobile platforms in a chosen geographical area can be readily constructed. The propagation information (e.g., time-varying and position-dependent path loss and carrier phase rotation) is extracted from the front-end tool and is used to control a matrix of Field-Programmable Gate Array (FPGA) based digital baseband channels. Each radio transmitter output is captured in real time, converted to a digital baseband signal, and passed through a digital baseband channel. The signal for each radio receiver is comprised of a linear combination of these digital baseband channel outputs. Each linear combination of channel outputs is converted to an analog RF signal and forms the input signal for a given radio receiver.

There are multiple challenges associated with the implementation of a digital real-time channel emulator. While digital emulation of a single radio channel is straightforward with today's FPGA technology, scaling this emulation to more than a few nodes requires careful attention to such issues as efficient node-to-node routing, minimization of digital path delays, synchronization among multiple analog front-ends, and real-time translation of front-end modeling tool output parameters to digital channel control values. We discuss our approaches to overcome these issues in the subsequent sections.

II. System Overview

A simplified block diagram of the TCES is shown in Figure 1. As currently configured, the system will support any heterogeneous combination of radios depending on the required operating frequency and bandwidth. Although the system is designed primarily to accept the RF output of a tactical radio, it can also accept the IF output of a modem or a baseband digital-to-analog converter (DAC) output. The system will also accept digital output signals with a straightforward modification to the interface. The overall system design emphasizes ease of growth and replication through the use of COTS equipment. As will be discussed, the design of the system permits flexible scaling to support operationally relevant scenario sizes. The RF / antenna port of each radio is connected through a cable to a signal conversion module (SCM). The SCM performs the conversion between analog RF signals and digital baseband signals. Signals are passed to and from the SCMs over high-bandwidth interconnects (HBI) that run between the SCMs and the digital channel emulator (DCE). The DCE is comprised of a COTS FPGA-based computing platform and MITRE-developed software and firmware that processes the digital baseband data.

The DCE performs digital emulation of multiple RF channels based on parameter sets generated using any of a variety of different RF modeling software packages. This enables coverage of several different layers of radio testing. At the fundamental level, radio performance as a function of SNR, minimum and maximum signal levels, co-channel and adjacent channel interference, and jamming can be evaluated. At the next level, receiver front-end functionality such as automatic gain control (AGC), demodulation, carrier tracking, and Doppler correction can be evaluated. Finally, the ability to place multiple radios in a simulated propagation environment enables complex MANET algorithms to be thoroughly tested and characterized prior to the low-rate initial production (LRIP) step of the acquisition process.

The outputs of the various channel prediction tools are translated by software running on a system control server into the necessary configuration commands to implement the desired channel characteristics in the DCE. The configuration commands are sent over Ethernet to the processing boards. Once the digital baseband signal passes through the channel modeling hardware, it is sent back to the SCMs, where it is converted back to RF and into the tactical radio's RF port. The TCES is implemented as a stand-alone rack as shown in Figures 2 and 3.

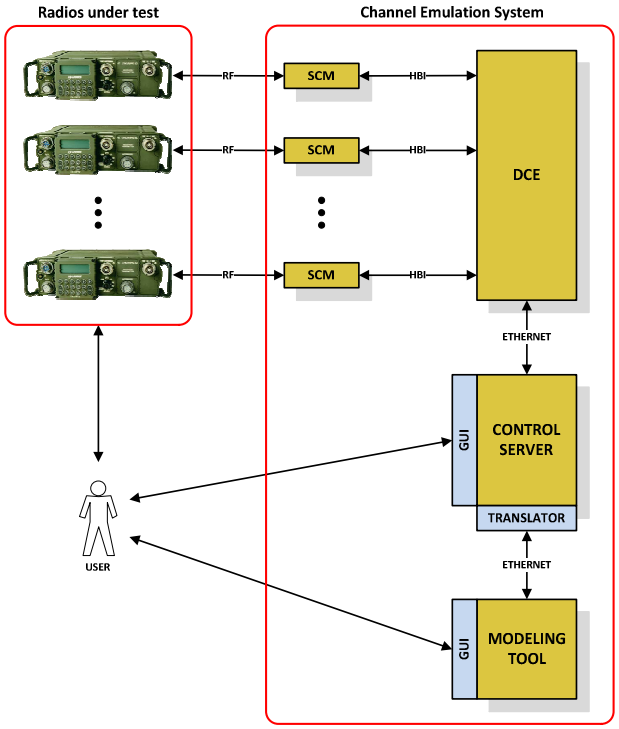

Figure 1. Simplified TCES Block Diagram

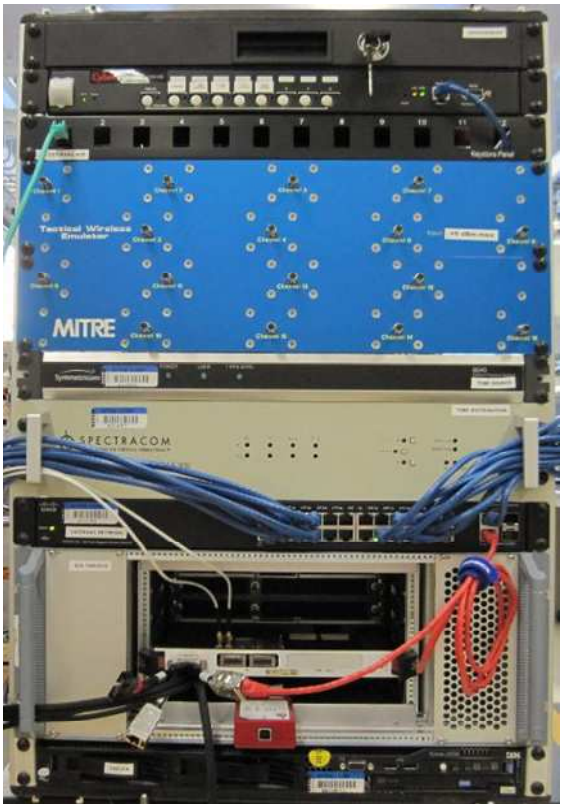

Figure 2. Front View of the TCES

Figure 3. Rear View of the TCES

The RF/antenna port of each radio to be tested is connected to the TCES front panel, where the transmit and receive signals of each radio are split into separate signal paths that connect to the RF input/output of one of the SCMs. A detailed view of the SCM signal chain is shown in Figure 4. On the receive side, the SCMs perform the downconversion from the RF frequency to a lower intermediate frequency (IF), which is then digitally filtered, further downconverted, and downsampled to produce complex baseband data with a signal bandwidth of 25 MHz. The samples are time stamped and sent over the HBI to the DCE for processing. The transmit side performs the reverse of these operations.

III. Implementation Details

There are a number of challenges associated with implementing a scalable system for multiple radio digital channel emulation. In order to accurately emulate the behavior of the RF channel across all nodes, it is necessary that all of the SCMs coherently sample the analog inputs across all radios. Each radio node interface requires an ADC and a DAC that must be time-synchronized in order to avoid phase errors (relative to the propagation-dependent phase rotations that the system needs to impart). Therefore, a rubidium oscillator is used to create a single timing reference that is distributed to all components in the system. Each component derives its necessary clocking signals from this global reference, which ensures that samples can be accurately time stamped, which simplifies the process of moving data throughout the system.

Another challenge is designing the system to provide for scalable hardware resources. Different channel models require different per-path resources, which limit the number of paths that can be emulated on any one board in the DCE. Additionally, the number of paths to be emulated increases as the square of the number of radios being tested, as the path between every pair of radios is potentially unique. Therefore, to support different channel models across systems of different size, the system architecture was designed to facilitate flexible partitioning across multiple FPGAs and boards.

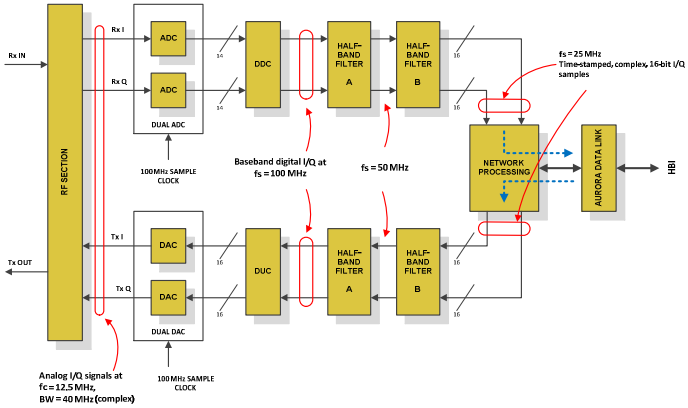

Figure 4. SCM Block Diagram

A further consideration is that the inherent delay of the system (through the various stages of processing such as sampling, up/down conversion, up/down sampling, filtering, etc.) imposes a lower limit on the point-to-point distance that can be emulated. One nanosecond of system delay translates into approximately one foot of emulated distance, so the system delay must be kept as low as possible to enable practical scenarios. Therefore, the system architecture must support flexible data movement between components, while minimizing the total introduced delay, which are goals that are often in opposition to each other.

One of the challenges with designing a system that can be flexibly split across multiple boards in a system is arranging the computations so that the FPGA I/O bandwidth is properly balanced to the logic resources. As each FPGA has limited logic resources and limited I/O capacity, the system must be designed ensure that the DCE implementation is not starved for data. In order to address this concern, the implementation utilizes a layered approach to abstraction to decouple the physical interfaces from the logical channels to support flexible partitioning. This and other related challenges will be discussed in the sections below.

A. SCM / Radio Interface Design

One important design goal of the system was to leverage COTS hardware, to the extent possible, to produce a system that is flexible, scalable, cost-effective, and easily reproduced.

The SCM of Figure 1 is based on a National Instruments N210 Universal Software Radio Peripheral with custom-developed FPGA logic. This low-cost software-defined radio (SDR) platform accepts RF interface daughter cards that cover frequencies from baseband up to 4.4GHz, which allow the system to interface to many relevant DoD and commercial radios. The RF front-end of the SCM downconverts the analog input signal to an IF of 12.5 MHz and digitizes it to 14 bits at 100 mega-samples per second (MSPS). The resulting complex IF signal is fed to a Xilinx Spartan-3A-DSP 3400 FPGA, where it is downconverted to baseband and transmitted serially to the DCE. The FPGA uses a Coordinate Rotation Digital Computer (CORDIC) based approach for downconversion. The CORDIC has a programmable frequency under the control of the SCM firmware. The baseband signal is filtered with a pair of half-band decimate-by-two low pass filters for an overall decimation rate of four (25 MSPS). On the transmit side, a digital-to-RF upconversion chain performs the reverse of the above processing steps to produce an RF signal corresponding to the output of each digitally emulated propagation channel. The MITRE system uses the commodity hardware with custom FPGA firmware to enable low latency digitization of the RF signal, and leverages the high speed serial data interface normally used for multi-input, multi-output (MIMO) applications. Our firmware uses the MIMO interface to transmit data directly to the DCE at a 2 Gbps line rate to support the sample bandwidth. Each SCM receives a reference clock, which enables distributed synchronization across the system. Sample alignment is maintained to within a few nanoseconds.

B. Digital Channel Emulation

The digital channel emulator (DCE) primarily models the wireless medium, and provides a flexible mechanism for imparting such propagation channel characteristics as path loss, phase shift, delay, multipath, and Doppler. The core of the digital channel emulation system is implemented using commercial OpenVPX FPGA boards. Our current implementation is based on the Curtiss-Wright HPE720 platform which features two Xilinx Virtex-5 SX240T FPGAs. The DCE can be easily configured to support multiple HPE720 boards depending on complexity of the channel and the size of the system. One of the challenges in multi-FPGA / multi-board designs is clock and time synchronization. To address this, a 10MHz reference clock and 1 pulse per second (PPS) signals are sent to a custom FPGA mezzanine card (FMC) card on the board and routed to the FPGAs. This ensures that each FPGA runs on the same clock and uses the correct timestamp. The HPE720 platform uses the Serial RapidIO (SRIO) protocol as the control plane. Host software configures FPGA hardware registers by way of serial rapid IO (SRIO) transactions delivered to the FPGAs from an on-board Power-PC (PPC) device. Logic resources in each FPGA decode these transactions and perform the appropriate register accesses. Serial data is transferred between the DCE and the SCMs by way of on-board multi-gigabit transceivers (MGT).

The DCE supports a user-defined *M*-by-*N* channel matrix, where *M* is the number of destination nodes and *N* is the number of source nodes. A given system configuration has a total of *MN* paths and each path consists of various logic subsystems, or "cells" that model different aspects of a given RF propagation channel. For example, a scale cell in each path accounts for signal attenuation. Other cells include integer and fractional sample delays cells and phase rotation cells. Additional cells are being developed to provide capabilities such as ray-traced and statistical multipath channel models. These latter models will enable the emulation of such features as correlated fading, an important consideration for MIMO. The cell-based architecture enables a flexible and parameterized design approach, whereby different standard channel models (in the form of pre-built FPGA firmware images) can be selected to satisfy tradeoffs between channel complexity and the number of radio nodes that can be accommodated. MITRE's current prototype implements a 12x12 system with integer (multiples of 40 ns) sample delays and complex amplitude scaling, or a 16x16 system with simple path loss on a single board.

C. Control Software and User Interface

The user interface and control software offer three methods for controlling the TCES hardware. The first is a simple interactive mode, whereby the user controls the channel characteristics of each path by entering values into a grid on a web form. The second is a scenario playback tool, where the user can upload a specially formatted file describing a time-varying scenario and play it back for easily repeating tests. The last is a JavaScript Object Notation (JSON)-based HTTP interface meant to be used for scripting emulator behavior or building custom user interfaces.

A major requirement for the design of the control software was loosely coupling scenario development tools such as STK or Remcom Wireless InSite and the control software. This allows the emulator to easily be integrated with existing test frameworks to expand capability. Simple scripts are provided to convert output from several modeling tools to the scenario file format mentioned above. If the modeling tool is capable of providing real-time updates, a simple software shim can be written to take output from the modeling tool and forward it to the emulator control software automatically. The emulator control software takes in values that describe RF channel characteristics, such as delay and path loss, and uses a modular architecture to simplify the creation of translators and filter plug-ins that perform the conversion from RF characteristics to raw control register values. Use of a pluggable architecture simplifies the process of adding new modeling cells and supporting new modeling tools. Each only requires a minimal amount of customized code that implements the desired translation. The supporting infrastructure takes care of the necessary housekeeping associated with the control plane flow.

IV. FUTURE WORK

We are working to extend our current prototype to incorporate such features as multipath and Doppler. Typical tactical radio stressing scenarios require less than 10 individual paths between each transmitter and receiver to account for signal multipath in challenging environments. Each path has its own associated delay, attenuation, phase rotation, and Doppler parameters. Given the large number of paths involved, along

with the need for independent fading coefficients on each path, an efficient implementation will be required. We believe that our system architecture facilitates the necessary tradeoffs.

As the achievable scale of the system is largely driven by the available hardware resources, the tradeoff between software and hardware implemented functionality is key. For example, by leveraging the channel modeling cell primitives that provide us with subsample delay and phase shift, we can support Doppler shifts without requiring additional hardware. By placing bounds on the emulated platform velocities, to bound the Doppler shift, we can realize the effects of Doppler through rapid software updates to the existing channel emulation cell control registers. Our control plane structures provide sufficient capacity to emulate Doppler shifts at closing speeds in excess of 300 miles-per-hour (MPH). While this may not be sufficient for aircraft, it is sufficient for many ground-based mobility scenarios, as well as some air-to-ground use cases. If modeling higher Doppler is necessary, custom cells can be added, with the understanding that there is a tradeoff between achievable system scale and complexity of channel model. However, as a single system can be easily reconfigured to support either case, the hardware can be effectively reused to answer different questions at different times.

V. CONCLUSION

A real-time digital baseband emulator of RF propagation channels has been developed and demonstrated [3]. The architectural features of this system enable a tradeoff between the number of radio nodes and the fidelity of the channel models. Further, the approach presented here results in a system that is scalable to an arbitrary number of radio nodes. The system that we have developed facilitates the testing of tactical radios to an extent not previously available, and is in current use by a DoD customer.

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